1 **TITLE of the INVENTION**

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3 Sense Amp Equilibration Device

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6 **CROSS-REFERENCE to RELATED APPLICATIONS**

7

8 Not applicable.

9

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11 **STATEMENT REGARDING FEDERALLY SPONSORED RESEARCH and**

12 **DEVELOPMENT**

13

14 Not applicable.

15

16

17 **BACKGROUND of the INVENTION**

18

19 1. Field of the Invention

20

21 This invention relates to monolithic dynamic random access memory array circuitry and,

22 more particularly, to techniques for sense amp equilibration.

23

24 2. Description of the Prior Art

25

26 Monolithic dynamic random access memory (DRAM) devices are well known. Within a

27 DRAM, data is transported between sense amp and array on a complementary-logic

28 bitline. After a read or refresh cycle, the complementary-logic bitline pairs are equilibrated

29 to match each other, and biased to a predetermined voltage so they can be properly read

30 by their sense amp in a future cycle.

31

32 During a read or refresh cycle, a selected data cell is connected to its bitline, raising or

33 lowering the bitline from its bias voltage. Its sense amp then senses the small voltage

34 difference between the new bitline level and its bias level, and amplifies that difference to a

35 full logic one or logic zero level. In this way, the infinitesimal charge of a tiny memory cell

36 is captured and presented to the rest of the chip and consequently to the outside world.

37 The charge of the data cell is also refreshed by the amplified voltage level on the bitline.

38 The bitline equilibration and bias circuitry is commonly considered to be part of the sense

39 amp circuitry.

40

41 It is also known that circuit area, sometimes called "real estate", is at a premium. The

42 smaller a device can be made, the faster it is likely to be, and more economical to

43 manufacture. Consequently, semiconductor engineers and mask designers all over the

44 world perpetually strive to reduce circuit size in order to stay cost competitive.

45

46 In a DRAM device, the memory array by far takes the most real estate. Second to the

47 memory array in size are the sense amps and related circuitry. Even a small area reduction

48 for a single sense amp is multiplied across all the sense amps, and chip size consequently

49 can be significantly reduced, thus improving cost competitiveness.

50

51 Blodgett, in patent US 6,466,499 B1, herein incorporated by reference, shows typical

52 DRAM technology, and is state-of-the-art, indicated by its very recent issue date of Oct.

53 15, 2002. Conventional three-transistor sense amp equilibrate and bias circuits are shown

54 as elements **50a** and **50b** in **FIGs 1, 2, 4, 5A, 5B**, and **5C.**

55

56 In Blodgett, equilibrate transistor **54** is gated by equilibrate signal **EQa** to short

57 complementary-logic bitlines **D0** and **D0*** together, thus equilibrating them. **EQa** also

58 gates bias transistors **56** and **58**, so that bias transistor **56** shorts bitline **D0** to node **Veq**,

59 and so that bias transistor **58** shorts bitline **D0*** to node **Veq**. **D0** and **D0*** are thus

60 biased to the voltage on node **Veq**.

62 For clarity and ease of comparison, in the present specification, prior art is represented in

63 the present application in **FIGs 1** and **2**. **FIG 1** is a typical prior art circuit schematic, and

64 **FIG 2** is that schematic represented in a layout. Because of the common and extensive use

65 in the industry of symmetry and reflected layouts for elegant design, four bitline pairs with

66 their relevant associated devices are shown in **FIG 2**.

67

68 In **FIGs 1** and **2**, **EQ** is the equilibrate signal gating equilibrate transistor **Q1**, and biasing

69 transistors **Q2** and **Q3**, **BL** and **BLn** are the complementary-logic bitlines, and the bias

70 voltage node is **Vbias**. When **EQ** is activated, equilibrate transistor **Q1** shorts **BL** and

71 **BLn** together (thus equilibrating them), and biasing transistor **Q2** shorts bitline **BL** to

72 biasing node **Vbias**, and biasing transistor **Q3** shorts bitline **BLn** to biasing node **Vbias**,

73 (thus biasing the bitlines).

74

75 Typical prior art as illustrated in **FIG 1** is deficient, in that with equilibrate transistor **Q1** in

76 the circuit, biasing transistors **Q2** and **Q3** are redundant with each other, wasting real

77 estate.

78

79 Further, as shown in **FIG 2**, the substrate contact for n-channels, referred to as **PPLUG**,

80 must be placed outside of the **QL** devices, thus increasing layout size. Also, the **Vbias**

81 contact needs to be placed outside of the source/drain of n-channel **Q3'** and **Q3''**, further

82 increasing the layout size, as represented by **L1**.

83

84 Zagar, in patent US RE35,825, herein incorporated by reference, is a prior art attempt to

85 avoid problems due to row-to-column shorts, and to reduce transistor count. There is no

86 equilibrate transistor, as that function is taken over by biasing transistors **QnA/QnB** being

87 activated simultaneously. As shown in Zagar **FIG 4**, four complementary-logic bitline

88 pairs **D1/D1*** through **D4/D4*** share a common current-limiting device **QL**. Each bitline

89 pair has biasing transistors **Q1A/Q1B** through **Q4A/Q4B**, connected in the conventional

90 way and gated by equilibrate node **EQ**. Instead of one current limiting device per bitline

91   pair, Zagar reduces area requirements by using one current limiting device **QL** per four

92   bitline pairs, which is gated permanently on, and biases the bitline pairs at the voltage on

93   node **DVC**.

94

95   Performance in Zagar is compromised because both **BL**s are shorted (equilibrated)

96   through two series n-channel transistors (**Q1A** and **Q1B**, for example), instead of through

97   a single transistor, thus doubling equilibrate time. Two series transistors of one width will

98   have half of the drive of a single transistor of the same width, hence slower equilibration

99   performance. The biasing speed is not as critical as the equilibrate speed. Zagar thus

100   reduces transistor count, but at the expense of slowing equilibration time.

101

102

103   **SUMMARY, OBJECTS, and ADVANTAGES of the INVENTION**

104

105   Disclosed herein is a new DRAM complementary-logic bitline equilibration and biasing

106   circuit, which has the distinct advantage of being implemented using less real estate than

107   prior art, thus lowering the manufacturing cost of the DRAM.

108

109   Specifically, this is accomplished by eliminating one of the bias transistors per bitline pair.

110   Said transistor has not been hitherto recognized as redundant.

111

112   This allows a smaller circuit layout which significantly reduces the area of sense amps and

113   related circuitry, while preserving identical control requirements and performance.

114

115

116   **DRAWING FIGURES**

117

118   List of Drawing Figures:

119

120	**FIG 1** shows a schematic of typical prior art bitline pair equilibrate and bias
121	circuitry.
122	
123	**FIG 2** shows a typical layout four bitline pairs using the circuit of **FIG 1**.
124	
125	**FIG 3** shows a schematic of the inventive bitline pair equilibrate and bias circuitry.
126	
127	**FIG 4** shows a layout of four bitline pairs using the inventive circuitry of **FIG 3**.
128	
129	List of Reference Numerals:
130	
131	**BL** is a logic-true side of a complementary-logic bitline pair.
132	**BLn** is a logic-inverse side of a complementary-logic bitline pair.
133	**EQ** is an equilibrate node/contact which carries an equilibrate signal and gates **Q1**,
134	**Q2**, and **Q3**.
135	**PPLUG** is substrate contact for n-channels.
136	**Q1** is an equilibrate transistor.
137	**Q2** is a biasing transistor.
138	**Q3** is a second biasing transistor.
139	**QL** is a current limiting device connecting biasing transistor(s) to **Vbias**.
140	**Vbias** is a biasing node/contact, holding a bias voltage between logic one and logic
141	zero.
142	**L1** is a representative length of a layout of the prior art circuit.
143	**L2** is a representative length of a layout of the inventive circuit.
144	
145	
146	**<u>DESCRIPTION and OPERATION of the PREFERRED EMBODIMENT</u>**
147	
148	Please refer to **FIGs 3** and **4**. **FIG 3** is a circuit schematic of the inventive circuit, and **FIG**
149	**4** is that schematic represented in a layout. Because of the common and extensive use in

150 the industry of symmetry and reflected layouts for elegant design, four bitline pairs with
151 their relevant associated devices are shown in **FIG 4**.

152

153 **BL** and **BLn** are bitlines in a typical complementary-logic bitline pair, within a typical
154 DRAM chip. Transistors **Q1** and **Q2** and current limiting device **QL** function as bitline
155 pair equilibrate and bias circuitry, the function of which is well-known in the art.

156

157 Equilibrate transistor **Q1** is gated by equilibrate node **EQ**, and is also connected to **BL**
158 and **BLn**, so that when **Q1** is activated by **EQ**, **BL** and **BLn** are shorted together through
159 **Q1**. Biasing transistor **Q2** is gated by equilibrate node **EQ**, and is also connected to **BL**
160 and to the drain terminal of current limiting device **QL**, so that when **Q2** is activated by
161 **EQ**, **BL** is shorted to **QL**. The source terminal of **QL** is connected to bias node **Vbias**.
162 **QL** is a resistive device well known in the art, such as a long-L transistor, and its function
163 is to limit current flow, so that if a bitline has a fault, **Vbias** is not depleted of charge and
164 is still able to bias healthy bitlines.

165

166 Equilibrate signal **EQ** gates equilibrate transistor **Q1**, and biasing transistor **Q2**. When
167 activated, equilibrate transistor **Q1** shorts **BL** and **BLn** together. And when activated,
168 biasing transistor **Q2** shorts **BL** to biasing node **Vbias** through current limiting device
169 **QL**. Because **Q1** and **Q2** are activated simultaneously, **BLn** is shorted to **BL**, which is
170 shorted to **Vbias** (through current limiting device **QL**), thus simultaneously equilibrating
171 and biasing both **BL** and **BLn**.

172

173 In all respects, the inventive is controlled the same as in prior art.

174

175 The difference between this circuit and prior art is that prior art uses two bias transistors,
176 **Q2** and **Q3** (as shown in **FIG 1**), and the inventive circuit uses only **Q2** (as shown in **FIG**
177 **3**), requiring less circuit area. Those familiar with the art had not hitherto recognized that
178 **Q2** and **Q3** are redundant with each other. Equilibration speed through **Q1** is identical to

179 prior art as shown in **FIG 1**, only now with reduced transistor count, and also better than

180 Zagar.

181

182 Referring to inventive layout in **FIG 4** in comparison to typical prior art in **FIG 2**, it can

183 be seen that the inventive elimination of **Q3** allows the shifting of bias node **Vbias**, into

184 the space vacated by the source terminal of former **Q3'** and **Q3"** of prior art, in an

185 interstitial and more compact fashion. **PPLUG** can now also be placed in the space

186 vacated by the drain terminal of former **QL** and **QL'** of prior art, next to the **QL** devices

187 instead of outside of them, as indicated by comparing **FIGs 2** and **4**.

188

189 The prior art layout of **FIG 2** has a representative length of **L1**. The inventive layout of

190 **FIG 4** has a representative length of **L2**. Because of the interstitial layout of **Vbias**

191 between **Q2'** and **Q2"**, and the n-channel substrate contact being next to the **QL** devices,

192 the inventive circuit results in a more compact design, as indicated by **L2** being

193 significantly smaller than **L1**, thus having reduced manufacturing cost.

194

195 For purposes of this application, in regard to layout, 'next to' refers to an orientation

196 wherein an element can be placed between duplicate equilibrating circuitry blocks,

197 allowing interstitial location between repeating blocks. This is illustrated in **FIG 4** of the

198 invention, where **Vbias** is 'next to' **Q1'**, which allows for interstitial location of **Vbias**

199 between repeating blocks, as evidenced by **Vbias** being interstitially located between **Q1'**

200 and **Q1"**. This is in contrast to 'outside of', which refers to an orientation which cannot be

201 interstitially oriented between repeating blocks, such as shown in **FIG 2** (prior art), where

202 **Vbias** is located 'outside of' devices **Q3'** and **Q3"**.

203

204 This is also illustrated in **FIG 2**, where prior art **PPLUG** is located 'outside of' the **QL**

205 devices, as compared to inventive **FIG 4**, where **PPLUG** is located 'next to' the **QL**

206 devices.

207

208

209 ## CONCLUSION, RAMIFICATIONS, and SCOPE

210

211 While there is shown and described the present preferred embodiment of the invention, it

212 is to be distinctly understood that this invention is not limited thereto but may be variously

213 embodied to practice within the scope of the following claims.

214

215 For example, bias transistor **Q2** can be connected to **BL** rather than **BLn**. The equilibrate

216 circuitry can be used in other sense amps not connected to **BL**s but to a data path, for

217 example, so by 'bitline pair', a data path is also circumscribed. The inventive circuitry is

218 also valid, independent of location of isolation devices between the array and sense amps:

219 that is, the inventive circuitry is valid on either side of array isolation devices. Adding a

220 two-terminal n-channel device in place of the three-terminal n-channel device **Q3** to

221 balance **BL** and **BLn** more closely will still be within the scope of the invention. Also,

222 current limiting device **QL** may or may not be required, depending on overall circuit

223 design of the chip. So when the **Vbias** node is indicated connected to a biasing voltage

224 circuit, a current limiting device may or may not be a part of that biasing voltage circuit. In

225 this case, **PPLUG** can then be located 'next to' **Vbias**, rather than **QL**, resulting in the

226 same inventive intent of reducing circuit length.

227

228 Clearly, other layouts may be conceived which express the reduced real estate

229 requirements of the inventive circuitry. Such layouts are expressions of the inventive

230 circuitry and are therefore within the scope of this invention. Also, though the above

231 description discloses many details, these details should not be understood to limit the

232 current invention. Obvious variations such as a minor change in logic design, addition of

233 passive devices, or a modified scheme for writing and reading data, while making use of

234 the structures, functions, or methods of the current invention, would fall within the scope

235 of the patent rights claimed by the inventor. Therefore the scope of the invention should

236 be limited only by the appended claims and their legal equivalents.

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